Claims

1. A receiver comprising:

a memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal from a plurality channels and outputs the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; and

a decoder, responsive to the data groups, which decodes the data samples within the data groups and outputs decoded data samples.

2. A receiver in accordance with claim 1 wherein:

the data samples each comprise orthogonally encoded data; and

the decoder is a biorthogonal inner code soft decision data decoder.

3. A receiver in accordance with claim 2 wherein:

the biorthogonal inner code soft decision data decoder is a Reed-Muller decoder.

4. A receiver in accordance with claim 2 wherein:

the orthogonally encoded data samples are QPSK encoded.

5. A receiver in accordance with claim 1 wherein:

the receiver is contained in a satellite.

6. A receiver in accordance with claim 2 wherein:

the receiver is contained in a satellite.

7. A receiver in accordance with claim 3 wherein:
the receiver is contained in a satellite.

8. A receiver in accordance with claim 4 wherein:
the receiver is contained in a satellite.

9. A receiver in accordance with claim 5 further comprising:
a channelizer, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

10. A receiver in accordance with claim 6 further comprising:
a channelizer, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

11. A receiver in accordance with claim 7 further comprising:
a channelizer, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

12. A receiver in accordance with claim 8 further comprising:

a channelizer, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

13. A receiver in accordance with claim 1 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

14. A receiver in accordance with claim 2 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

15. A receiver in accordance with claim 5 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and

the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

16. A receiver in accordance with claim 9 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

17. A method of data reception comprising:

receiving and storing a time division multiplexed signal containing a sequence of data samples from a plurality of channels;

outputting the stored data samples in a sequence of data groups, each data group containing a plurality of samples from one of the plurality of channels;

decoding the data samples within each data group; and

outputting the decoded data samples of the plurality of data groups.

18. A method in accordance with claim 18 wherein:

the data samples each comprise orthogonally encoded data; and

the decoder is an inner code soft decision biorthogonal decoder.

19. A method in accordance with claim 18 wherein:

the orthogonally encoded data samples are QPSK encoded.

20. A method in accordance with claim 17 wherein:

the data is received by a satellite.

21. A method in accordance with claim 18 wherein:

the data is received by a satellite.

22. A method in accordance with claim 19 wherein:

the data is received by a satellite.

23. A method in accordance with claim 20 wherein:

an input bandwidth is received and is divided with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

24. A method in accordance with claim 21 wherein:

an input bandwidth is received and is divided with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

25. A method in accordance with claim 22 wherein:

an input bandwidth is received and is divided with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

26. A method in accordance with claim 17 wherein:

the data samples are stored in an addressable storage array containing memory cells which are addressed by a pair of addresses, the sequence of data samples being written in a group of memory cells each containing one common address of the pair of addresses and the sequence of data groups are each individually outputted from a group of memory cells containing one common address which is another of the pair of addresses.

27. A method in accordance with claim 18 wherein:

the data samples are stored in an addressable storage array containing memory cells which are addressed by a pair of addresses, the sequence of data samples being written in a group of memory cells each containing one common address of the pair of addresses and the sequence of data groups are each individually outputted from a group of memory cells containing one common address which is another of the pair of addresses.

28. A method in accordance with claim 20 wherein:

the data samples are stored in an addressable storage array containing memory cells which are addressed by a pair of addresses, the sequence of data samples being written in a group of memory cells each containing one common address of the pair of addresses and the sequence of data groups are each individually outputted from a group of memory cells containing one common address which is another of the pair of addresses.

29. A method in accordance with claim 23 wherein:

the data samples are stored in an addressable storage array containing memory cells which are addressed by a pair of addresses, the

sequence of data samples being written in a group of memory cells each containing one common address of the pair of addresses and the sequence of data groups are each individually outputted from a group of memory cells containing one common address which is another of the pair of addresses.